What is claimed is:

1. A memory cell array, comprising:

a plurality of memory transistors arranged in a two-dimensional array wherein the two-dimensional array is defined by a first direction and a second direction, each memory transistor having two source/drain regions arranged in a first direction of the memory cell array with a channel substrate region therebetween, and a gate structure arranged above the channel substrate region,

said source/drain regions and channel substrate regions being formed in a substrate arranged on an insulating layer, and the channel substrate regions of memory transistors adjacent each other in the first direction being separated from each other by respective source/drain regions extending down to the insulating layer,

wherein

said source/drain regions and channel substrate regions of memory transistors adjacent each other in a second direction of the memory cell array are isolated from each other by trenches filled with insulating material and formed in the substrate so as to extend down to the insulating layer.

2. A memory cell array according to claim 1,
wherein the source/drain regions and the channel substrate regions are formed in the silicon layer of an SOI wafer.

3. A memory cell array according to claim 1,

wherein the gate structure of the memory transistors consists of a layer sequence comprising an insulating gate layer, a floating gate on the insulating gate layer, an intermediate dielectric on the floating gate and a control gate on the intermediate dielectric.

4. A memory cell array according to claim 3, further comprising word lines connected in electrically conductive manner to control gates of a row of memory transistors arranged in said second direction.

5. A memory cell array according to claim 4, further comprising bit lines, with a respective row of memory transistors arranged in the first direction having first and second bit lines associated therewith and the source/drain regions of the memory transistors of the row being connected in electrically conducting manner to the first bit line and the second bit line in alternating fashion.

6. A memory cell according to claim 5, further comprising a means for introducing charges to the floating gate of a selected memory transistor of the memory cell array, which applies a potential of a first polarity, at which a channel is formed in the channel substrate region, to the word line connected to the control gate of the selected memory transistor, and applies a potential of a second polarity opposite to said first polarity to one of the source/drain regions of the selected memory transistor in order to bring charges to the floating gate of the selected memory transistor.

7. A memory cell array according to claim 6, wherein said means for introducing charges furthermore applies a potential of said first polarity to one of the source/drain regions of the memory transistors -

excluding the selected memory transistor - having their control gates connected to the word line that is connected to the control gate of the selected memory transistor.

8. A memory cell array according to claim 7, further comprising a means for removing charges from the floating gate of a selected memory transistor, which applies a potential of said second polarity to the word line connected to the control gate of the selected memory transistor and applies a potential of said first polarity to both source/drain regions of the selected memory transistor in order to remove charges from the floating gate of the selected memory transistor.

9. A memory cell array according to claim 8, wherein said means for removing charges furthermore applies a potential of said second polarity to the source/drain regions of the memory transistors - excluding the selected memory transistor - having their control gates connected to the word line that is connected to the control gate of the selected transistor.

10. A method of making a memory cell array, comprising the steps of:

forming strip-shaped trenches, filled with insulating material, in a semiconductor substrate arranged on an insulating layer, said insulating trenches extending down to the insulating layer;

forming strip-shaped gate structures which extend substantially perpendicularly to the trenches filled with insulating material and, together with said trenches, constitute a grid-like structure; and doping the substrate regions left free between the grid-like structure so as to form source/drain regions extending down to the insulating layer.

11. A method according to claim 10, further comprising the steps of:

forming word lines on the gate structures; and

forming bit liens, with a first and a second bit line each being associated with a row of source/drain regions arranged in the direction of the trenches filled with insulating material, and the source/drain regions being connected in alternating fashion to said first and second bit lines.